

Remarks

In view of the foregoing amendments and following remarks responsive to the Office Action of December 20, 1994, Applicant respectfully requests favorable reconsideration of this application.

In section 1 of the Office Action, the Examiner asked Applicant to provide the serial number of the co-pending application listed on page 11. Applicant has amended the specification accordingly.

In section 2 of the Office Action, the Examiner objected to the disclosure stating, on page 17, line 19, output data 106 is not found in Figure 6. The Examiner's objection is well taken. The output of de-serializer 122 described on page 17, lines 15 through 19, is labelled 104a in the figure. The specification has been amended accordingly.

The Examiner also asserted that it is unknown if the circuit 58 depicted in Figure 7 is the same as controller 58 of Figure 2. It is the same element. It is believed that the specification and reference numerals are clear on this point and that no amendments are necessary.

Finally, the Examiner stated that after page 46, the pages containing Tables VIII-X are not numbered. Applicant has amended the specification to label these sheets as page numbers 47 through 51.

In section 3 of the Office Action, the Examiner rejected all pending claims, claims 1-14 and 16-18, under 35 U.S.C. §112, second paragraph, as being indefinite.

Specifically, with respect to claim 1, the Examiner stated that the connection between the claimed elements is not clear. Applicant has amended claim 1 to more expressly recite the connections between the elements.

The Examiner also asserted with respect to claim 1, that the reference to "means for determining" is not clear and that nothing is disclosed that corresponds to such means. Applicant respectfully traverses. The "means for determining... whether said data output by said deserializer is to be provided to said receive memory means" as recited in newly amended claim 1 comprises, for instance, demultiplexer 1304 (see, page 22, lines 12-16, page 23, lines 12-25, and page 25, line 34 - page 26, line 9). The means for determining may also be considered to include receive control block 1218, frame differentiator 1216 and 16-bit walking 1-counter 1219 (see, page 25, line 34 - page 26, line 9, specifically). The operation of the means for determining is clearly described in the above-noted passages of the specification. Accordingly, this rejection should be withdrawn.

The Examiner also rejected claim 1 under 35 U.S.C. §112, second paragraph, asserting that it is unknown if the parallel data recited in claim 1 is from the transmit memory means. This objection is not understood. Claim 1, lines 12-14 clearly recite that the parallel data is the output from the deserializer. Accordingly, it is not from the transmit memory means. The claim is clear as to the source of the parallel data and this rejection should be withdrawn.

With respect to claim 1, the Examiner further asks whether the control signals of line 4 are transmitted on the medium. As described on page 21, lines 30-34, the control signals are generated by receive path control unit 1218. These control signals may or may not be generated as a result of information transmitted on the medium. However, the

above-referenced description on page 21, however, is merely that of a preferred embodiment of the invention. Applicants do not wish to limit the claim to embodiments in which the control signals are or are not transmitted over the medium. Since the Examiner has cited no prior art which would require Applicant to so limit the claims, the source of the control signals is not a required claim limitation and need not be added to claim 1.

Finally with respect to claim 1, the Examiner stated that "memory means" lacks clear antecedent basis. Applicant has amended the claim to overcome this rejection. Accordingly, claim 1 now meets all requirements under 35 U.S.C. §112.

With respect to claim 3, the Examiner stated that "said data" and "the status port activities" lack antecedent basis. Applicant has amended claims 1 and 3 in order to overcome this rejection.

With respect to claim 4, the Examiner stated that the coupling between the claim elements is not clear and, moreover, it is unknown what is meant by "the status of interrupts".

Applicant has amended claim 4 to more clearly recite the coupling between the claimed elements. Applicant has also amended claim 4 to now recite "a status of interrupts" to avoid any antecedent basis issues. As to what is meant by "status of interrupts", the Examiner is referred to page 22, line 17 - page 23, line 11. In that part of the specification, it describes that interrupt data from other physical layer devices are stored in a register bank 1222. Accordingly, there should be no confusion as to what is meant by "status of interrupts".

The Examiner also stated that an unclear description of the coupling also appears in claims 5-

14 and 16-18. Applicant has amended the claims where appropriate to more particularly recite the coupling of the claimed elements.

With respect to claim 9, the Examiner stated that it is not clear if the data stations of line 4 are identical to the data stations recited in the preamble of claim 1. Applicant has amended claim 9 to clearly distinguish between the "network data stations" and the "data stations". Particularly, in the terminology of claim 9, network data stations are a type of data station.

Concerning claim 9, the Examiner also stated that the recitation in lines 2-6 that the first and second network data stations and the other data stations were coupled to the same transmission media is not supported by the specification because the backbone transmission medium connecting the hubs is different from the medium connecting stations to a hub. Applicant respectfully traverses. In the terminology of claim 9, the term "medium" encompasses both mediums. Since both mediums together comprise an overall communication medium, the claim is in accordance with acceptable and normal claiming practices and is not indefinite. Accordingly, the rejection of claim 9 under 35 U.S.C. §112 should be withdrawn.

With respect to claim 11, the Examiner stated that the means for determining has no input. Applicant respectfully traverses. There does not appear to be any need to recite the source of input data, if any, to the means for determining. Accordingly, this rejection should be withdrawn.

The Examiner also listed certain specific objections with respect to claim 16. Applicant has

herein cancelled claims 16 and 17, thus making these rejections moot.

Finally under 35 U.S.C. §112, second paragraph, the Examiner rejected claim 18, stating that it is unknown how the apparatus of line 8 is connected to other elements such as the communications medium and the first and second network data stations. The Examiner also stated that the reference to the FIFO buffer is not clear because nothing is disclosed that corresponds to the FIFO buffer connected to a data station. Finally, the Examiner stated that the receive memory has no output and the transmit memory has no input.

With respect to the connection of the elements, Applicant has amended claim 18 to more specifically recite the various connections. With respect to the FIFO buffer recited on line 16, the Examiner's attention is drawn to element 1432 in Figure 14 and the description on page 25, lines 6-20 and the even more detailed description in the middle of page 31 through the top of page 37. Accordingly, the FIFO is adequately disclosed.

As to the output of the receive memory and the input of the transmit memory, as discussed above with respect to claim 11, there appears to be no need under the patent statute to recite those connections.

In section 5 of the Office Action, the Examiner rejected claims 1, 2 and 7 under 35 U.S.C. §102(b) as being anticipated by Hamada, et al. (Hamada)]. The Examiner did not reject the other claims, claims 3-14 and 16-18, based on any prior art grounds. With respect to claims 1, 2 and 7, the Examiner stated that Hamada discloses a transmission system including buffers 2120 and 2124 (receive and transmit memories), a receive data path and a transmit data

path, a time slot controller 21, 22 (a processor for outputting control signals), and a receive data transfer controller (means for determining). The Examiner also stated that the receive data path includes a serial/parallel converter 2119 (a deserializer), and the transmit path has a parallel/serial converter 2125.

Applicant respectfully traverses. The Hamada reference relates to a token ring type network in which the order of connection of the various data stations can be rearranged to cause a source and destination station to be positioned closer to each other (in serial order). The present invention, on the other hand, relates to a star-type topology network in which all data links are point to point.

In Hamada, the relevant circuitry appears in Figure 7 and is part of the node data stations, such as station 21. Hamada's datapath receives a single stream of data on line 3 and demultiplexes it for presentation to a plurality of data devices 4, 11 and 12.

In the present invention, on the other hand, while data is demultiplexed to change it from serial to parallel in each line of the received datapath 12, the purpose of the receive datapath is to combine the multiple data lines in order to fill a single buffer 132. Accordingly, the present invention is essentially performing the opposite function (many-to-one time multiplexing) as Hamada (one-to-many demultiplexing). Thus, although the present invention and Hamada may appear, at first glance, to be similar, they are quite different.

Nevertheless, the Examiner's position is understood in that claim 1 was not drafted to specifically emphasize this distinction between the

present invention and Hamada. However, original claim 1 did clearly distinguish over Hamada and has herein been amended to even more clearly distinguish over Hamada. Particularly, claim 1 recites, "means for selectively transmitting, in response to one of said plurality of control signals, said data output by said deserializer to said receive memory means." As recited in claim 1, data is selectively provided from each line of the receive datapath to the buffer 132 depending on appropriate control signals from the processor. In Hamada, on the other hand, the received data is always stored in buffer 2120. The receive data transfer controller 2121 determines, not whether or not the data is stored in buffer 2120, but where the data is sent to from the output of buffer 2120. Accordingly, Hamada does not teach selectively transmitting data to the receive memory means responsive to a control signal as claimed.

Accordingly, claim 1 distinguishes over Hamada. Claims 2 and 7 depend from claim 1 and, therefore, also distinguish over Hamada.

In view of the foregoing amendments and remarks, this application is now in condition for allowance. Applicant respectfully requests the Examiner to issue a Notice of Allowance at the earliest possible date. The Examiner is invited to contact Applicant's undersigned counsel by telephone call in order to further the prosecution of this case in any way.

Respectfully submitted,

LIMBACH & LIMBACH

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By

Theodore Naccarella

Theodore Naccarella
Reg. No. 33,023

Attorneys for Applicant

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